

REMARKS

Applicants respectfully request entry of the foregoing amendments and reconsideration of the merits of the outstanding rejections in view of the following remarks. Claims 1-44 are currently pending. In this Reply, claims 8, 18, 28, and 37 have been amended. The amendments to the claims were made solely to improve their form, readability, and/or clarity and were not made to distinguish the claimed subject matter over the cited references. No new matter has been added.

I. Prior Art Rejections

Claims 1, 4-8, 12, 13, 16-18, 22, 23, 26-28, 32, 33, 36-38, 42, and 43 stand rejected under 35 U.S.C. § 102(b), as allegedly being anticipated by U.S. Patent No. 5,768,598 to Marisetty, *et al.* ("Marisetty").¹ See 6/14/04 Office Action, page 2. Further, claims 9-11, 19-21, 29-31, and 39-41 stand rejected under 35 U.S.C. § 103(a), as allegedly being unpatentable over Marisetty in view of Applicants' specification. See *id.* at page 4. Moreover, claims 2, 3, 14, 15, 24, 25, 34, 35, and 44 stand rejected under 35 U.S.C. § 103(a), as allegedly being unpatentable over Marisetty in view of U.S. Patent No. 6,483,903 to Itay *et al.* ("Itay").² See *id.* at page 5. Applicants respectfully traverse these rejections on the following grounds.

A. The Anticipation Rejection of Claims 1, 4-8, 12, 13, 16-18, 22, 23, 26-28, 32, 33, 36-38, 42, and 43

Under 35 U.S.C. § 102, the Patent Office bears the burden of presenting at least a *prima facie* case of anticipation. *In re Sun*, 31 USPQ2d 1451, 1453 (Fed. Cir. 1993) (unpublished). Anticipation requires that a prior art reference disclose, either expressly or under the principles of inherency, each and every element of the claimed invention. *Id.* In addition, the prior art reference must be enabling. *Akzo N.V. v. U.S. International Trade Commission*, 808 F.2d 1471, 1479, 1 USPQ2d 1241, 1245 (Fed. Cir. 1986), *cert. denied*, 482 U.S. 909 (1987). That is, the prior art reference must sufficiently describe the claimed invention so as to have placed the

¹ The Office Action appears to incorrectly identify the Marisetty patent as U.S. Patent No. 5,792,598. The Marisetty patent relied upon is believed to be U.S. Patent No. 5,768,598.

² The Office Action appears to incorrectly identify the Itay patent as U.S. Patent No. 6,580,752. The Itay patent relied upon is believed to be U.S. Patent No. 6,483,903.

public in possession of it. *In re Donohue*, 766 F.2d 531, 533, 226 USPQ 619, 621 (Fed. Cir. 1985). Such possession is effected if one of ordinary skill in the art could have combined the publication's description of the invention with his own knowledge to make the claimed invention. *Id.* That is, the prior art reference must sufficiently describe the claimed invention so as to have placed the public in possession of it.

With regard to independent claims 1, 13, 23, and 33, the Examiner asserts that Marisetty discloses each and every recited limitation. Particularly, the Examiner contends that Marisetty's bus lines 112 (referring to Fig. 1 and col. 5, ll. 37-39) are equivalent to or comprise a general purpose input/output (GPIO) line as recited in each independent claim. *See* 6/14/04 Office Action, page 2 and 6. Applicants respectfully disagree and maintain that the Examiner's reasoning is unsoundly based.

1. Marisetty's Bus Lines Are Not GPIO Lines

Marisetty's bus lines 112 and the claimed GPIO lines function fundamentally different and are not equivalent. A general purpose input/output line or "GPIO line" is a term of art that refers to a bidirectional line that can be configured as either an input or an output line. *See, e.g.*, Applicants' Specification, paragraph 2. The configuration of a GPIO line can vary, *i.e.*, a GPIO line can be configured as an input line at one time and then configured as an output line at another time or vice-versa. *See generally* independent claims 1, 13, 23, and 33. However, it is well known in the art that bus lines are statically configured in a unidirectional manner, *i.e.*, signals always travel in the same direction along a bus line. Bus lines are not directionally reconfigured. In sum, Marisetty's bus lines 112 are not GPIO lines. Because Marisetty does not disclose a GPIO line, which is a limitation recited in all independent claims, Marisetty fails to anticipate claims 1, 13, 23, and 33, and all claims dependent therefrom (*i.e.*, claims 4-8, 12, 16-18, 22, 26-28, 32, 36-38, 42, and 43).

2. Marisetty's Fails to Provide Adequate Specificity

Even assuming, *arguendo*, that Marisetty's bus lines 112 comprise a line that could in theory function in a similar manner as a GPIO line, Marisetty fails to sufficiently describe the claimed invention so as to have placed the public in possession of it. For example, independent claim 1 recites that "providing, using [one] GPIO line, a first input from a first circuit component to the integrated circuit during a first time [and] providing, using [the same] GPIO line, a first output from the integrated circuit to a second circuit component during a second time."

Emphasis added. Independent claims 13, 23, and 33 recite similar limitations. In other words, one GPIO line can serve as an input line at one time and then as an output line at another time. Yet, Marisetty does not disclose this sort of reconfiguration for any of the cited bus lines 112 relied upon by the Examiner. Rather, Marisetty merely discloses a shared logic block (CLB) 103A, which can be reconfigured by interruption signals according to the specification of a particular I/O device. *See* Marisetty, col. 5, ll. 48-54. Simply put, Marisetty does not disclose configuring one of the bus lines 112 as an input line at one time and an output line at another time. Because Marisetty fails to provide adequate specificity vis-à-vis the claimed limitations, Marisetty fails to anticipate independent claims 1, 13, 23, and 33, and all claims dependent therefrom.

3. Other Dependent Claims Are Clearly Novel

Dependent claims 7, 17, and 27, recite or similarly recite “wherein the step of providing a first input comprises the step of configuring the GPIO line as an input line during a portion of the first time, and the step of providing a first output comprises the step of configuring the GPIO line as an output line during the second time.” Marisetty fails to disclose this sort of dynamic reconfiguration. *See* Remarks § I.A.2, *supra*.

Dependent claims 8, 18, 28, and 37 recite or similarly recite “wherein: the portion of the first time includes a first predetermined sequence of processing cycles; and the second time includes a second predetermined sequence of processing cycles different from the first sequence.” Support for this limitation can be found at least at paragraph 24 of Applicants’ Specification. Marisetty fails to disclose line reconfiguration at predetermined times, *i.e.*, after specified intervals. *See* Remarks § I.A.1 and 2, *supra*. Rather, Marisetty’s system is based on the use of interrupts generated spontaneously by the I/O devices. *See* Marisetty, abstract.

For at least the reasons set forth above, Applicants contend that the rejection of claims 1, 4-8, 12, 13, 16-18, 22, 23, 26-28, 32, 33, 36-38, 42, and 43 is improper. Applicants respectfully request the Examiner to withdraw the instant rejection.

B. The Obviousness Rejection of Claims 2, 3, 14, 15, 24, 25, 34, 35, and 44

As stated in MPEP § 2143, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation

of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). Further, as stated in MPEP § 2143.01, to establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). That is, "[a]ll words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 165 USPQ 494, 496 (CCPA 1970). Finally, if an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

With respect to dependent claims 2, 3, 14, 15, 24, 25, 34, 35, and 44, the Examiner acknowledges that Marisetty "fails to teach the first component is further adapted to provide the first input at a low frequency relative to the switching frequency of the GPIO line and that the first time is concurrent with the second time." 6/14/04 Office Action, page 5. In an attempt to cure this deficiency, the Examiner introduces Itay as allegedly teaching "a method and system in a DSL environment wherein a first component is adapted to provide the first input at a low frequency relative to the switching frequency of the GPIO line and that the first time is concurrent with the second time." *Id.* The Examiner then concludes that "[it] would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the method and system of Marisetty with the teachings of Itay such that the first component is further adapted to provide the first input at a low frequency relative to the switching frequency of the GPIO line and that the first time is concurrent with the second time in order for multi-channel communications can occur along the same lines simultaneously as suggested by Itay." *Id.* Applicant respectfully disagrees.

Itay does not teach "a first component is adapted to provide the first input at a low frequency relative to the switching frequency of the GPIO line and that the first time is concurrent with the second time" as the Examiner suggests. Itay discloses a DSL system implementing telephone lines 12, not GPIO lines that are found in integrated circuits. Clearly, telephone lines are not GPIO lines. Itay does not cure the deficiency noted with respect to

Marisetty. Accordingly, Marisetty, either taken alone or in combination with Itay, fails to teach all of the recited limitations found in claims 2, 3, 14, 15, 24, 25, 34, 35, and 44.

Moreover, dependent claims 2, 3, 14, 15, 24, 25, 34, 35, and 44 depend from either independent claim 1, 13, 23, or 33. Itay does not cure the deficiencies of Marisetty noted with respect to independent claims 1, 13, 23, and 33. *See* Remarks § I.A, *supra*. Applicants submit that the rejection of dependent claims 2, 3, 14, 15, 24, 25, 34, 35, and 44 is improper and respectfully request the Examiner to withdraw the instant rejection.

C. The Obviousness Rejection of Claims 9-11, 19-21, 29-31, and 39-41

Dependent claims 9-11, 19-21, 29-31, and 39-41 depend from either independent claim 1, 13, 23, or 33. Itay does not cure the deficiencies of Marisetty noted with respect to independent claims 1, 13, 23, and 33. *See* Remarks § I.A, *supra*. Applicants submit that the rejection of dependent claims 9-11, 19-21, 29-31, and 39-41 is improper and respectfully request the Examiner to withdraw the instant rejection.

II. Conclusion

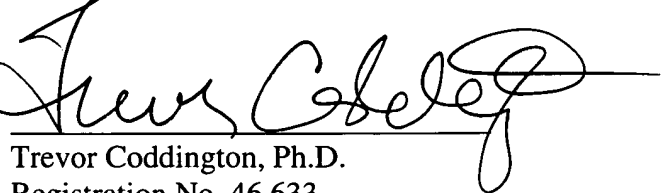
In view of the foregoing, it is respectfully submitted that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number, in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

No fee is believed to be necessary for entry and consideration of this Reply. In the event that the United States Patent & Trademark Office requires a fee to enter and consider the instant Reply or to maintain the application pending, please charge or credit such variance to the undersigned's Deposit Account No. 50-0206.

Respectfully submitted,

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